REMARKS

In a "Notice of Panel Decision from Pre-Appeal Brief Review," mailed on August 24, 2007, the Office maintained the rejection of claims 1-3, 6-10, 12-17, 20-14, 26-31, 34-38, 40-45, 48-52, and 54-56.

By this Amendment, filed concurrently with a Request for Continued Examination, Applicant cancels claims 43-45, 48-52, and 54-56 without prejudice or disclaimer of the subject matter thereof. All of the computer-readable apparatus claims have been canceled. Thus, the rejection of these claims under 35 U.S.C. § 101 is now moot.

In addition, by this Amendment, Applicant requests a telephone interview with the Examiner prior to the next Office communication.

The only remaining rejection in this application is the rejection of claims 1-3, 6-10, 12-17, 20-14, 26-31, 34-38, 40-42 under 35 U.S.C. § 102(b) based on Verbauwhede et al. (U.S. Pat. No. 5,710,914). As explained earlier, taking claim 1 as being exemplary, Verbauwhede does not teach "executing the first instruction during both of its first and second execution states, in which a first at least one of an arithmetic operation, a logical operation, an address calculation operation, a masking operation, and a shifting operation of the first instruction is performed in response to first source operand information, and in which first destination operand information is output in response thereto ... and executing the second instruction during a selected one of its first and second execution stages, in which a second at least one of an arithmetic operation, a logical operation, an address calculation operation, a masking operation, and a shifting operation of the second instruction is performed in response to second source operand information, ... so that the second instruction is executed: during only its first execution stage in response to the second source operand information being independent of the first destination operand information; and during only its second execution stage in response to the second source operand information being dependent on the first destination operand information ... ," as recited in claim 1. In particular, claim 1 requires that the second instruction be executed during a selected one of the first and second execution stages depending on whether the second source operand information is independent of the first destination operand information or not. Verbauwhede has no teachings related to this aspect of the claimed subject matter.

Instead, Verbauwhede teaches a conventional instruction pipeline that has only one execute stage. (*See* FIG. 4; col. 6, l. 65 to col. 7, l. 10). Only during this single execute stage any operations on operands are performed. The Examiner believes that the "Read" stage of Verbauwhede is equivalent to one of the execution stages recited in claim 1. Applicants

respectfully disagree. No operation, such as an arithmetic operation, logical operation, address calculation operation, masking operation, or shifting operation is performed during the "Read" stage of Verbauwhede. Instead, data is simply read from a memory location. As explained in Verbauwhede: "[d]uring the Read cycle, data is read from one or two locations within data memory 6." There is no teaching whatsoever of an operation, such as an arithmetic operation, a logical operation, an address calculation operation, a masking operation, or a shifting operation being performed during the "Read" stage of Verbauwhede. Thus, the "Read" stage of Verbauwhede cannot be equated to an execution stage, as claimed.

Moreover, as explained above, claim 1 requires that the second instruction be executed during a selected one of the first and second execution stages depending on whether the second source operand information is independent of the first destination operand information or not. Verbauwhede has no teachings related to this subject matter. As explained above, since Verbauwhede teaches only one execution stage, no selection between two execution stages is (or can be) taught by Verbauwhede. The Examiner points to col. 10, lines 42-60 of Verbauwhede to conclude that Verbauwhede teaches this limitation. The cited portion of Verbauwhede, however, merely teaches the notion of a data hazard that can occur during execution of instructions by the pipeline described in Verbauwhede. In particular, in the Verbauwhede pipeline the read cycle of instruction i+1 occurs after the write cycle of instruction i. So, in case instruction i+1 was programmed to read the result of instruction i, then instruction i+1 may read incorrect data. This is because instruction i+1 would read a memory location that does not have the result of instruction i yet. In sum, instruction i+1 would end up operating on wrong data. Verbauwhede, however, does not teach that the second instruction be executed during a selected one of the first and second execution stages depending on whether the second source operand information is independent of the first destination operand information or not. Instead, Verbauwhede teaches that "the programmer should avoid storing in program memory 4 a sequence of instructions that would give rise to such a hazard." (col. 11, ll. 59-60). In particular, Verbauwhede teaches away from the claimed invention by stating that the programmer should not store, in the memory, instruction i+1 subsequent to instruction i, where i+1 depends on the result of instruction i, since that would cause a data hazard.

In contrast to the teachings of Verbauwhede, the claims are directed to addressing the data hazard problem by requiring that the second instruction be executed during a selected one of the first and second execution stages depending on whether the second source operand information is independent of the first destination operand information or not. Thus, consistent with the present invention, programmer can store instruction i+1 immediately subsequent to

instruction i, even if instruction i+1 depends on the result of instruction i, since the present invention can execute such instructions using different execution stages in such a way that the hazard mentioned in Verbauwhede does not occur.

Indeed, the Examiner notes in the Final Office Action that the instructions in Verbauwhede "follow a pipeline and thus cannot skip a stage in a pipeline." (*See* Final Office Action, page 6, last sentence of first paragraph). Thus, an instruction in Verbauwhede cannot be executed during a selected one of the first and second execution stages depending on whether the second source operand information is independent of the first destination operand information or not since that would be tantamount to skipping a stage in the pipeline. Contrary to the teachings of Verbauwhede, Applicant teaches the skipping of stages in a pipeline. (*See* Specification, FIG. 7, which shows stages in the pipeline being skipped). Thus, Applicant respectfully submits that Verbauwhede fails to teach "executing the first instruction during both of its first and second execution states, in which a first arithmetic operation of the first instruction is performed in response to first source operand information, and in which first destination operand information is output in response thereto … and executing the second instruction during a selected one of its first and second execution stages, in which a second arithmetic operation of the second instruction is performed in response to second source operand information, … so that the second instruction is executed: during only its first execution stage in response to the second source operand information being independent of the first destination operand information; and during only its second execution stage in response to the second source operand information being dependent on the first destination operand information," as recited in claim 1.

Accordingly, because Verbauwhede does not teach each and every limitation of claim 1, claim 1 is patentable over the cited reference.

Claims 2, 3, 6-10, and 12-14 depend, directly or indirectly, upon claim 1 and thus are patentable for at least the reasons given above with respect to claim 1.

Applicant respectfully submits that claim 15 is patentable for similar reasons as given above with respect to claim 1, because Verbauwhede does not teach assembling the first instruction for execution during both of its first and second execution stages, in which a first arithmetic operation of the first instruction is to be performed in response to first source operand information, and in which first destination operand information is to be output in response thereto; and assembling the second instruction for execution during a selected one of its first and second execution stages, in which a second arithmetic operation of the second instruction is to be performed in response to second source operand information, … so that the second

instruction is to be executed: during only its first execution stage in response to the second source operand information being independent of the first destination operand information; and during only its second execution stage in response to the second source operand being dependent on the first destination operand information, as recited in claim 15.

Claims 16, 17, 20-24, and 26-28 depend, directly or indirectly, upon claim 15 and thus are patentable for at least the same reasons as given above concerning claim 15.

Applicant respectfully submits that claim 29 is patentable for similar reasons as given above with respect to claim 1, because Verbauwhede does not teach first circuitry and second circuitry for performing the method recited in claim 1.

Claims 30, 31, 34-38, and 40-43 depend, directly or indirectly, upon claim 29 and thus are patentable for at least the same reasons as given above concerning claim 29.

Accordingly, Applicant respectfully requests the Examiner to withdraw the rejection of pending claims 1-3, 6-10, 12-17, 20-24, 26-31, 34-38, 40-42 under 35 U.S.C. § 102(b) as being anticipated by Verbauwhede. The Final Office Action contains numerous statements characterizing the claims, the Specification, and the prior art. Regardless of whether such statements are addressed by Applicant, Applicant refuses to subscribe to any of these statements, unless expressly indicated by Applicant. Should issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the Applicant's representative at (512) 996-6839.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

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